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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,067	REGNIER, JOHN W.	
	Examiner	Art Unit	
	Magid Y Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002 and 08 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-25 and 31* is/are allowed.

6)☒ Claim(s) *1-4,10-12,26-29,32-34 and 37* is/are rejected.

7)☒ Claim(s) *5-9,13-16,30,35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

2.

The oath or declaration is defective because:

It does not identify the citizenship of each inventor.

Claim Objections

3. Claim 13 is objected to because of the following informalities: in claim 13, line 2, delete "11" and insert --12--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 4, 10 – 12, 26 –29, 32 – 34 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,805,860 to Parham.

6. Referring to claim 1, Parham teaches a computer implemented method and system for extracting flat data from a hierarchical representation of a circuit (see Abstract; column 1, lines 5 – 25) comprising: (a) a processing sequence that selects elements during a traversal of a hierarchical representation of a circuit (Abstract; col. 3, lines 6 – 50); (b) a processing sequence that determines if flat data for the data has been previously stored (Fig. 21, blocks 628 and 630); and (c) a processing sequence which if flat data has been previously stored, appends previously stored data to an accumulated flat data that is hierarchically and traversably related to the selected element (Figs. 11 – 25). Thus, Parham discloses all the elements of the claim.

7. As per claims 2, 3, 4,10 and 11 see (6) above, and flow charts depicted on Figs. 16 – 25, which disclose all the claimed limitations pertaining to flat and hierarchical data representations and traversal of hierarchy.

8. Referring to claim 12, Parham recites a computer implemented system for extracting flat data from a hierarchical representation of a circuit comprising: (a) a flat data structure for storing a flat data segment when an instance of a cell is initially

encountered during traversal of a hierarchical representation (see above; Fig. 21); (b) a processing sequence for selecting a cell instance from the hierarchical representation (Fig. 21); (c) a processing sequence for determining if a selected cell instance has a matching flat path segment stored (Figs. 21 – 23); and (d) a processing sequence for retrieving flat data for the cells (see above; Fig. 25). Parham thus cites all the limitations of the claim.

9. Referring to claim 26, Parham discloses a computer implemented system for extracting flat data from a hierarchical representation of a circuit comprising: (a) means for selecting elements of a hierarchical representation of a circuit and determining flat data for a selected element (see above; col. 4, lines 1 – 45); (b) means for identifying repetitive cell instance elements of the hierarchical representation (col. 20, line 65 to col. 21, line 12); (c) means for storing flat data for the selected element and accumulated flat data segments (see above; Figs. 24 and 25); (d) means for identifying selected cell element (see above; col. 3, line 5 to col. 4, line 45); and (e) means for retrieving the flat data segment for the selected element and appending the retrieved flat data segment (see Figs. 115 – 25).

10. Claim 27 contains the same limitations as claim 3, and therefore the same rejections apply.

11. Claims 28 and 29 contain the same limitations as claim 1, and thus the same rejections apply.

12. Referring to claim 32, Parham cites a method for extracting and storing reusable flat data from a hierarchical netlist (Abstract) comprising: (a) selecting a cell instance not encountered during netlist traversal (Figs. 21 – 24); (b) determining a flat path data describing elements along a net within the selected cell from the cell instance upper level hierarchy boundary point (see above; Figs. 15 – 25); (c) storing the flat path data segment (see above); and (d) retrieving a stored sequence of flat data segment, assembling the flat data segment, and storing the flat data segment (see Figures cited above). Parham thus discloses all the elements of the claim.

13. As per claim 33, Parham teaches a method for generating flat data from a hierarchical circuit design comprising: (a) selecting a first element within the hierarchy that has not been processed (see above); (b) if the first element is a cell, storing an identifier for the first element (see Figs. 23 and 24); and (c) storing flat data describing flat data path (see above; Fig. 25; col. 21, line 12 to col. 22, line 52).

14. As per claim 34, see above; col. 19, lines 45 – 67 which show how to determine if a selected element has an identical identifier as an element listed in the data structure, as claimed.

15. Referring to claim 37, Parham cites a method for extracting flat data from a hierarchical representation of a circuit, comprising: (a) selecting a first element of a hierarchical representation of a circuit (see above); (b) determining if the first element has the same flat data as a previously selected element, and if it is retrieving the stored flat data (Abstract; col. 3, lines 6 - 50); and (d) combining and storing a copy of the retrieved flat data path segment with a cumulatively combined flat data containing a sequence of flat data path segments (see above; Figs. 18, 19, 20, 21, 22).

Allowable Subject Matter

16. Claims 17 – 25 and 31 are allowed.

17. Claims 5 – 9, 13 – 16, 30 and 35 – 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter: these claims contain various elements pertaining to a method and system for extracting and generating flat data from a hierarchical representation of a circuit that are not cited or suggested in the prior art of record.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,684,376 to Kerzman et al cites a method and apparatus for efficiently selecting cells within a circuit design database which includes four primary features for selecting cells including (a) selecting only cells in a pre-defined region and selection area; (b) maneuvering through the circuit design hierarchy and selecting cells or regions at selected levels of hierarchy by using predetermined up and down hot-keys; and (c) sorting selected cells by instance name or net name.

Pub. No. US 2004/0078767 to Burks et al discloses a method for modeling IC designs in a hierarchical design automation system that utilizes a block abstraction, including a set of all database objects (cells, nets, wires, vias and blockages) that are necessary to achieve accurate placement, routing, extraction, simulation, and verification of the block's ancestors in the hierarchy.

U.S. Patent No. 6,668,362 to McIlwain et al teaches a method and apparatus for hierarchical verification for equivalence checking of designs that use compare points in the two designs to be compared and verified, and also teaches the traversal of the hierarchy in the invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
22 June 2004